

FORM PTO-1449 (SUBSTITUTE)		Attorney Docket No.: M&N-IT255 Appl. No.	
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		Applicant KARL SCHROEDINGER ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))		Filing Date November 16, 2001 Group Art Unit JC857 U.S. PTO 09/992281 2816 11/16/01	

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
<i>lun</i>	A	5,015,872	05/91	Rein	327	231	
	B						
	C						
	D						
	E						
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	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
	J						
	K						
	L						
	M						
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

<i>lun</i>		Thomas H. Lee et al.: "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM", IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, December 1994, pp. 1491-1496;

EXAMINER <i>lun</i>	DATE CONSIDERED <i>01/24/2003</i>
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.